REMARKS

In the Office Action, the Examiner noted that claims 1-22 are pending in the application and that claims 1-22 are rejected. By this response, all claims continue unamended.

In view of the following discussion, the Applicants submit that none of the claims now pending in the application are obvious under the provisions of 35 U.S.C. §103. Thus, the Applicants believe that all of these claims are now in allowable form.

Relections

A. 35 U.S.C. § 103

The Examiner rejected claims 1-5 under 35 U.S.C. §103(a) as being unpatentable over Lindberg (U.S. Patent No. 6,366,579) in view of Sharony et al (U.S. Patent No. 5,495,356, hereinafter "Sharony"). The rejection is respectfully traversed.

The Examiner alleges that regarding claims 1-5 Lindberg discloses in Figs. 11-12 a space/time switching unit wherein the data words in the received time slots are disassembled to bit level such that each data word is divided into a number of bits, BIT0 to BIT7. The Examiner further alleges that each bit is then distributed to a respective row of speech stores SS of that row. The Examiner further alleges that the multiplexers, 8/1 MUXs, controlled by the associated control stores, CS, are operative to output selected bits from the speech stores. The Examiner concedes however, that Lindberg does not disclose an apparatus for conveying said selected bit pack to any output data position within a combination of output data rails and time slots. As such, the Examiner cites Sharony for disclosing a system in which an input and/or N inputs are connected to a passive broadcast medium that broadcasts an input and/or all the inputs to each one or all N outputs. Thus the Examiner alleges that it would have been

obvious to one having ordinary skill in the art to include the apparatus of Sharony in the system of Lindberg. The Applicants respectfully disagree.

The Applicants respectfully submit that the teachings of Lindberg or Sharony, alone or in any allowable combination do not teach, suggest or make obvious the invention of the Applicants, at least with respect to claims 1-5. More specifically, the Applicants' claim 1 specifically recites:

> "Apparatus for switching data from any of a plurality of inputs to any of a plurality of outputs, said data formatted as data blocks containing a fixed number of bits of data, each data block comprising "O" bit packs containing a number of bits "P", where O and P are integers, said apparatus comprising:
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> apparatus for receiving a plurality of respective input bit packs organized in a combination of input data rails and time slots,
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> apparatus for selecting any of the respective input bit packs from any of the rails in any of the time slots, and
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> apparatus for conveying said selected bit pack to any output data position within a combination of output data rails and time slots."
> (emphasis added).

In support of the Applicants' invention, at least with respect to Applicants' claim 1 above, the Applicants, in the Specification, specifically recite:

> "In accordance with the principles of the illustrative embodiment, when the switch module 130 receives a data block, e.g. a byte, the disassembler 140 slices the data block into bit-packs, e.g. bits, and distributes the bits to the various switching cores 150-158. Consequently, all the respective bit ones, twos, threes, fours, fives, six, sevens, and eights from data channels input to the disassembler 140 are respectively routed to the switching core 150, 152, 154, 156, . . . 158." (See Specification page 7, lines 13-18).
>
> "Within each switching core 150-158 all the relevant bits (e.g., bit 1's for switch module 130, bit 2's for switch module132, etc.) are illustratively input to the switching core on 16 rails in 48 time slots (note that 16x48=768). Each rail is carrying data at the rate of 311.04 Mb/s. In this manner, the data rate of 768 STS-1 signals can be accommodated by 8 such devices. That is, since the transmission rate of an STS-1 signal is 51.84 megabits per second (Mbps), 768 such signals would yield a

transmission rate of 39.81 Gigabits per second (Gbps). Because each device's switching core operates on one bit of each of the 768 channels in parallel, with each bit being processed at a rate of (number of rails per switching core) X (number of switching cores)X(switch processing speed) = 16 X 8 X 311.04 Mbps = 39.81 Gbps, the data rate of 768 STS-1 signals." (See Specification page 11, lines 8-17).

As evident from at least the excerpts of the Applicants' specification recited above, the Applicants' invention is directed, at least in part, to advantageously performing switching on respective individual pit packs of an input data signal in parallel.

The Examiner concedes that Lindberg fails to teach, suggest or make obvious an apparatus for conveying said selected bit pack to any output data position within a combination of output data rails and time slots. The Applicants agree. However, the Applicants submit that Lindberg further fails to teach, suggest or make obvious, at least respective switching as taught in the Applicants' Specification and claimed by at least the Applicants' claim 1 recited above. More specifically, in contrast to the invention of the Applicants, at least with respect to claims 1-5, Lindberg, as pointed out by the Examiner, specifically recites:

"The subrate switch SRS comprises a matrix of speech stores SS, and associated multiplexors and control stores. However, the speech stores SS in the subrate switch SRS are prepared to store bits instead of entire words in the storage positions. The subrate switch SRS is further equipped with an input terminal IN and an output terminal OUT. The time slots that are provided to a predetermined input terminal of the TS-module XMB is also distributed to the input terminal IN of the subrate switch SRS such that the subrate switch SRS is continuously supplied with time slots. In the subrate switch SRS, the data words in the received time slots are disassembled to bit level such that each data word is divided into a number of bits BIT0 to BIT7. Each bit is then distributed to a respective row of speech stores in the subrate switch SRS, and stored in all speech stores SS of that row. The multiplexors 8/1 MUXs controlled by the associated control stores CS are operative to output selected bits from the speech stores. The selected output bits of the multiplexors 8/1 MUX in the subrate switch SRS are combined in a bits-to-word converter into an entire

word which is sent to the TS-module XMB." (See Lindberg, col. 18, lines 41-48).

In the invention of Lindberg, at least with respect to the embodiment of FIG. 11, a received data word is disassembled to bit level such that each data word is divided into a number of bits BIT0 to BIT 7. Each of the bits is then distributed to and stored in all of the speech stores of a respective row. The multiplexors 8/1 MUXs then output selected bits from the speech stores **in column format**. More specifically, in Lindberg, each bit is stored in all of the speech stores of a respective row. That is, BIT0 of a data word is stored in all of the speech stors one of row; BIT1 is stored in all of the speech stores of row two, BIT3 is stored in all of the speech stores in row three...and so on. Multiplexors in Lindberg then select a bit from column one, a bit from column two...for all of the columns.

In contrast, in the invention of the Applicants, a data block is disassembled into bit components, e.g., BIT1 to BIT8. All of the BIT1s of the data blocks received in the Invention of the Applicants are communicated to a first switch module and are routed to first switching core. As such, the first switching core of the Applicants' invention switches only the BIT1s of the data blocks, which is in contrast to the invention of Lindberg. As such the Applicants' invention is able to switch signals with much higher data rates. For example in one embodiment of the Applicants' invention, because each device's switching core operates on one bit of each of 768 channels in parallel, with each bit being processed at a rate of (number of rails per switching core) X (number of switching cores)X(switch processing speed) = 16 X 8 X 311.04 Mbps, the Applicants' invention is able to switch signals having data rates as high as 39.81 Gbps, the data rate of 768 STS-1 signals. The invention of Lindberg does not teach, suggest or make obvious the respective and parallel switching of the Applicants' invention as taught in the Applicants' Specification and claimed in at least the Applicants' claim 1. For at least the reasons stated above and as conceded by the Examiner, the Applicants respectfully submit that the teachings of Lindberg,

alone, fail to make obvious the invention of the Applicants, at least with respect to claim 1.

Furthermore, the Applicants respectfully submit that the Sharony reference alone also fails to teach, suggest or make obvious the invention of the Applicants, at least with respect to claims 1-5. The Applicants respectfully submit that there is absolutely no teaching, suggestion or disclosure in Sharony for at least an "apparatus for receiving a plurality of respective input bit packs organized in a combination of input data rails and time slots" or for an "apparatus for selecting any of the respective input bit packs from any of the rails in any of the time slots" as taught in the Applicants' specification and claimed by at least the Applicants' claim 1. The Applicants' invention is directed, at least in part, to a switch that receives respective bit packs (i.e., respective bit ones, twos, threes, fours, fives, six, sevens, and eights) of the input data and switches the respective bit pack to any output data position within a combination of output data rails and time slots.

> "In accordance with the principles of the illustrative embodiment, when the switch module 130 receives a data block, e.g. a byte, the disassembler 140 slices the data block into bit-packs, e.g. bits, and distributes the bits to the various switching cores 150-158. Consequently, all the respective bit ones, twos, threes, fours, fives, six, sevens, and eights from data channels input to the disassembler 140 are respectively routed to the switching core 150, 152, 154, 156, . . . 158." (See Specification page 7, lines 13-18).
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> "Within each switching core 150-158 all the relevant bits (e.g., bit 1's for switch module 130, bit 2's for switch module132, etc.) are illustratively input to the switching core on 16 rails in 48 time slots (note that 16x48=768). Each rail is carrying data at the rate of 311.04 Mb/s. In this manner, the data rate of 768 STS-1 signals can be accommodated by 8 such devices. That is, since the transmission rate of an STS-1 signal is 51.84 megabits per second (Mbps), 768 such signals would yield a transmission rate of 39.81 Gigabits per second (Gbps). Because each device's switching core operates on one bit of each of the 768 channels in parallel, with each bit being processed at a rate of (number of rails per switching core) X (number of switching cores)X(switch processing speed)

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= 16 X 8 X 311.04 Mbps = 39.81 Gbps, the data rate of 768 STS-1 signals." (See Specification page 11, lines 8-17).

As evident from at least the excerpts of the Applicants' specification recited above, the Applicants' invention is directed, at least in part, to advantageously performing switching on respective individual pit packs of an input data signal in parallel.

In contrast, Sharony teaches a switching network that utilizes at least three degrees of freedom, time, wavelength and space. In one embodiment of Sharony, each space channel between an input and an output is assigned a time slot and wavelength coordinate characteristic of the output and the input transmitter and output receiver are tuned to the appropriate time and wavelength coordinates and selective switching is used to complete the space channel between the input and output. In another embodiment of Sharony, each input channel is assigned a set of space, time slot and wavelength coordinates and an input signal is broadcast to all of the outputs which selectively makes connection to those inputs with an appropriate set of coordinates. (See Sharony, Abstract). In contrast to the Applicants' invention, however, Sharony specifically teaches:

"The STSW has two stages, the first stage shown in FIG. 3 is composed basically of n mxm star couplers 31 and the second stage shown is composed of m nxln Wavelength-Time Selective Switches 32 (WTSSs). The two stages are connected to each other by mn optical links 33, that may be optical fibers. To each one of the n star couplers 31, m optical transmitters 34 are connected, each fixed with a different wavelength (e.g., .lambda..sub.0, .lambda..sub.1, ...lambda..sub.m-1). Each optical transmitter 34 is driven by an electrical signal composed of l inputs multiplexed in time (e.g., t.sub.0,t.sub.1, . . . t.sub.l-1) by a time division multiplexer 35. Thus, each input channel space is uniquely identified by a triplet indicating the fixed sub-channels it uses in each of the three dimensions, i.e., (s.sub.i, .lambda..sub.j, t.sub.p). Each WTSS 32 has In outputs and it receives the entire information from all the N inputs." (See Sharony, col. 5, lines 46-60). (emphasis added).

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In the invention of Sharony, each of the WTSS receives the entire information from all the N inputs. The invention of Sharony does not, and further, is not capable of performing the switching taught and claimed by the Applicants' invention. More specifically, the invention of Sharony does not teach, suggest or disclose a switch comprising an "apparatus for receiving a plurality of respective input bit packs organized in a combination of input data rails and time slots" or for an "apparatus for selecting any of the respective input bit packs from any of the rails in any of the time slots" as taught in the Applicants' specification and claimed by at least the Applicants' claim 1. The invention of Sharony does not teach performing the switching of data separated into bit packs wherein the bit packs are respectively switched (i.e., each bit pack is switched in parallel by a respective switch.)

Furthermore, the Applicants submit that there is absolutely no suggestion or motivation in any of the references to combine the teachings of Lindberg and Sharony as suggested by the Examiner.

For prior art reference to be combined to render obvious a subsequent invention under 35 U.S.C. § 103, there must be something in the prior art as a whole which suggests the desirability, and thus the obviousness, of making the combination. Uniroyal v. Rudkin-Wiley, 5 U.S.P.SQ.2d 1434, 1438 (Fed. Cir. 1988). The teachings of the references can be combined only if there is some suggestion or incentive in the prior art to do so. In re Fine, 5 U.S.P.SQ.2d 1596, 1599 (Fed. Cir. 1988). Hindsight is strictly forbidden. It is impermissible to use the claims as a framework to pick and choose among individual references to recreate the claimed invention Id. at 1600; W.L. Gore Associates, Inc., v. Garlock, Inc., 220 U.S.P.Q. 303, 312 (Fed. Cir. 1983).

Moreover, the mere fact that a prior art structure could be modified to produce the claimed invention would not have made the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992); In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

The Applicants further submit that even if a suggestion to combine the references as suggested by the Examiner did exist (which the Applicants submit that no such suggestion exists), the Examiner's attention is directed to the fact that the alleged references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious the Applicants' invention, at least with regard to the Applicants' independent claim 1. The substantial gap between the teachings of Lindberg and the invention of the Applicants is not bridged by the teachings of Sharony. More specifically, the combination of the teachings of Lindberg and Sharony fail to teach, suggest or make obvious at least an "apparatus for receiving a plurality of respective input bit packs organized in a combination of input data rails and time slots" or for an "apparatus for selecting any of the respective input bit packs from any of the rails in any of the time slots" as taught in the Applicants' specification and claimed by at least the Applicants' claim 1. That is, as described above, the Lindberg fails to teach, suggest or make obvious the respective bit switching of the Applicants' invention at least with respect to the Applicants' claim 1. Furthermore, the teachings of Sharony fail to teach, suggest or make obvious the respective bit switching of the Applicants' invention at least with respect to the Applicants' claim 1. As such, any allowable combination of the Lindberg and Sharony reference also fail to teach, suggest or make obvious the respective bit switching of the Applicants' invention at least with respect to the Applicants' claim 1.

Therefore, the Applicants respectfully submit that claim 1, as it now stands, fully satisfies the requirements of 35 U.S.C. § 103 and is patentable thereunder.

Likewise, independent claims 5, 6, 11, 16 and 20 recite similar relevant features as recited in claim 1. As such, and for at least the reasons stated herein, the Applicant submits that Lindberg and Sharony, alone or in any allowable combination, do not teach, suggest or make obvious independent claims 5, 6, 11, 16 and 20, and that independent claims 5, 6, 11, 16 and 20 as

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they now stand, also fully satisfies the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Furthermore, dependent claims 3-4, 7-9, 12-14, 17-19 and 21-22 depend either directly or indirectly from independent claims 1, 6, 11, 16 and 20 and recite additional limitations therefore. As such and for at least the reasons set forth above, the Applicant submits that none of these claims are obvious with respect to the teachings of Lindberg and Sharony, alone or in any allowable combination. Therefore, the Applicant submits that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

The Applicants reserve the right to establish the patentability of each of the claims independently in subsequent prosecution.

B. 35 U.S.C. § 103

The Examiner has rejected claims 6-22 under 35 U.S.C. § 103 as being unpatentable over Sharony in view of Lindberg. The rejection is respectfully traversed.

The Examiner alleges that regarding claims 6 -22, Sharony discloses in Fig. 3, a multidimensional switching network for broadcasting any of the input data to a plurality of output channels. However, the Examiner correctly concedes that Sharony does not disclose wherein the data is formatted as data blocks containing a fixed number of bits of data, each data block comprising "O" bit packs containing a number of bits "P", where O and P are integers. As such, the Examiner cites Lindberg for teaching such limitations.

For at least the reasons recited above with respect to the Examiner's rejection of claims 1-5 of the Applicants' invention, the Applicants further submit that the teachings of Sharony and Lindberg, alone or in any allowable combination, fail to teach, suggest or make obvious the invention of the Applicants at least with respect to claims 6-22.

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More specifically, the Applicants' claims 6-22, much like the Applicants' claims 1-5, are directed, at least in part, to a switching core for switching respective bits of a data block. As recited above, the teachings of Sharony and Lindberg, alone or in any allowable combination fail to teach, suggest or make obvious the respective bit switching as taught by the Applicants' Specification and claimed in at least the Applicants' claims 6-22.

Therefore and for at least the reasons stated above, the Applicants respectfully submit that independent claims 6, 11, 16 and 20 as they now stand, fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Furthermore, dependent claims 7-9, 12-14, 17-19 and 21-22 depend either directly or indirectly from independent claims 6, 11, 16 and 20 and recite additional limitations therefore. As such and for at least the reasons set forth above, the Applicant submits that none of these claims are obvious with respect to the teachings of Lindberg and Sharony, alone or in any allowable combination. Therefore, the Applicant submits that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

The Applicants reserve the right to establish the patentability of each of the claims independently in subsequent prosecution.

Conclusion

Thus, the Applicants submit that none of the claims presently in the application are obvious under the provisions of 35 U.S.C. § 103. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending n the application, it is requested that the Examiner telephone Jorge Tony Villabon, Esq. at (732) 530-9404 x1131 or Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate

arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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